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EXAMINER	
ELLIS, RICHARD L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,110	VAN DYKE ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-72 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4,8-14,18-22,24-36,38-44,46,49,52-63 and 65-72 is/are rejected.

7)☒ Claim(s) 5-7,15-17,23,37,45,47,48,50,51 and 64 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2,5,6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-72 presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

3. Claim 26 is rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3.1. The scope of meaning of the following terms are unclear:

3.1.1. "designed to process the RISC instructions independently a point within a recipe of a CISC instruction at which the RISC instruction was generated" claim 26; From the wording of this portion of the claim, it appears that one or more words may have been omitted between the words "independently a".

4. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

6. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

7. Claim 1 is rejected under 35 USC § 102(b) as being clearly anticipated by Blomgren et al., U.S. Patent 5,685,009, incorporating by reference Blomgren et al., U.S. Patent 5,781,750 at col. 3 lines 43-47.

Blomgren et al. (009) and Blomgren et al. (750) were cited in applicant's information

disclosure statement, paper number 2, received February 26, 2001.

Blomgren et al. (009) and Blomgren et al. (750) taught (e.g. see figs. 1-8 of Blomgren et al. (009) and 1-3 Blomgren et al. (750)) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

7.1. a computer (Blomgren et al. (009) col. 1 lines 23-25) comprising;

7.2. a RISC instruction decoder (Blomgren et al. (009) col. 1 lines 39-44, Blomgren et al. (750) fig. 2, "RISC ID") exposed for execution of user-state programs in a RISC instruction set (Blomgren et al. (009) col. 1 lines 39-42), being an instruction set having fixed-length instructions and a load/store/operate organization (this is the inherent definition of a RISC instruction set), and;

7.3. a hardware CISC instruction decoder (Blomgren et al. (009) col. 1 lines 37-40 and 42-45, Blomgren et al. (009) fig. 2, "CISC ID") exposed for execution by user-state programs in a CISC instruction set (Blomgren et al. (009) col. 1 lines 37-40), being an instruction set with variable-length instructions and many instructions having multiple side-effects (this is the inherent definition of a CISC instruction set, see also Blomgren et al. (750) at col. 9 lines 1-4), the CISC decoder designed to decode a portion of an instruction set for the computer (Blomgren et al. (009) col. 3 lines 60-67, Blomgren et al. (750) col. 5 lines 13-20 and 48-67 and col. 9 lines 4-7, 23-33, and 56-63), and to deliver the decoded instructions to an instruction execution pipeline (Blomgren et al. (750) fig. 2, 48, col. 7 lines 1-12) designed to execute the output of both the RISC instruction decoder and the CISC instruction decoder (Blomgren et al. (750) fig. 2);

7.4. a software emulator programed to implement a remainder of the instruction set (Blomgren et al. (009) col. 3 lines 57-67, Blomgren et al. (750) col. 4 lines 21-33);

7.5. the CISC instruction set providing accessibility to only a subset of the registers of the general register file (Blomgren et al. (009) col. 15 line 30 to col. 16 line 50), intermediate results of instructions of the instruction set being stored in registers of the

general register file that are inaccessible in the CISC instruction set (Blomgren et al. (009) col. 17 lines 24-29).

8. Claims 2-4, 8-14, 18, 32-34, 36, 39-44, 46, and 56-63, are rejected under 35 USC § 102(b) as being clearly anticipated by Blomgren et al., U.S. Patent 5,685,009, incorporating by reference Blomgren et al., U.S. Patent 5,781,750 at col. 3 lines 43-47.

As to claim 2, Blomgren et al. (009) taught:

8.1. decoding instructions of a user-state program coded in a RISC instruction set (Blomgren et al. (009) col. 1 lines 39-42) in a hardware instruction decoder of a computer (Blomgren et al. (009) col. 1 lines 39-44, Blomgren et al. (750) fig. 2, "RISC ID"), the RISC instruction set being an instruction set having fixed-length instructions and a load/store/operate organization (this is the inherent definition of a RISC instruction set); and,

8.2. decoding instructions of a user-state program coded in a CISC instruction set (Blomgren et al. (009) col. 1 lines 37-40) in a CISC hardware instruction decoder of a computer (Blomgren et al. (009) col. 1 lines 37-40 and 42-45, Blomgren et al. (009) fig. 2, "CISC ID"), the CISC instruction set being an instruction set having variable-length instructions and many instructions having multiple side-effects (this is the inherent definition of a CISC instruction set, see also Blomgren et al. (750) at col. 9 lines 1-4), and;

8.3. the instructions decoded by the CISC decoder and RISC decoder being executed in a common execution pipeline (Blomgren et al. (750) fig. 2, 48).

9. As to claim 3, Blomgren et al. (009) taught that the pipeline exception circuitry was designed to recognize an exception occurring in a CISC instruction after a first side-effect of the CISC instruction has been architecturally committed, and thereupon, to expose an instruction pointer, contents of a general register file, and contents of processor registers to a software exception handler (col. 15 line 30 to col. 16 line 50), the processor registers and

general purpose registers of the computer exposing sufficient processor state and providing sufficient working storage for execution of the exception handler and resumption of the program, without recomputing the first side-effect, without storing processor state to the main memory (col. 9 lines 30-54, col. 14 lines 1-42 and col. 17 lines 24-29).

10. As to claim 4, Blomgren et al. (009) taught a register and control logic (col. 14 lines 22-24) for that register designed to capture and expose an intra-instruction program counter value when a CISC instruction raises an exception at an intermediate point (col. 14 lines 22-34).

11. As to claims 8-14, 18, 28-36, 38-44, 46, 49, 52-63, and 65-72, they do not teach or define above the invention claimed in claims 1-4 and are therefore rejected under Blomgren et al. (009) and Blomgren et al. (750) for the same reasons set fourth in the rejection of claims 1-4, supra.

12. As to claims 8, 18, 49, and 65, Blomgren et al. (750) taught that as a result of execution of a program in the CISC instruction decoder, the instruction opcode calling for a memory reference to effect a movement of data, performing a memory protection check effective to check for permission to effect a movement of data other than the data movement called for by the instruction opcode (col. 6 lines 1-13).

13. As to claim 12, Blomgren et al. (009) taught an exception handler for initiation by an exception occurring at an intermediate point during execution of one of the instructions of the first instruction set (col. 14 lines 1-3), the exception handler being coded in the RISC instruction set (col. 14 lines 1-3) having accessibility to the registers inaccessible in the CISC instruction set (col. 16 lines 37-42), any saving of the intermediate results as part of a save of machine state using mechanisms used for saving general registers (col. 14 lines 9-15).

14. As to claim 28, Blomgren et al. (009) taught that the RISC instruction set had a condition-code based compare and branch repertoire (col. 1 lines 33-42).

15. As to claim 29, Blomgren et al. (009) taught that the RISC instruction set includes designators into a unified register file designed to contain integer and floating-point data

(Blomgren et al. (750) fig. 2, 50), and the CISC instruction set includes designators into distinct integer and floating-point register files (col. 1 lines 38-40, where the x86 has distinct integer and floating-point register files).

16. As to claim 30, Blomgren et al. (009) taught that intermediate results of multiple-side-effect instructions in the CISC instruction set are held in temporary registers of the computer (col. 17 lines 24-30) that are not explicitly designated in the representations of the CISC instructions themselves (col. 16 lines 24-26), and instructions of the RISC instruction set include designators into a register file, the RISC register designators including designators to the temporary registers used in the CISC instruction set (col. 16 lines 38-50).

17. As to claim 31, Blomgren et al. (750 taught a memory management unit (fig. 2, 52) designed to manage the instructions of the RISC and CISC instruction sets between a main memory of the computer and one or more cache levels (col. 5 lines 49-55, col. 9 line 65 to col. 10 line 32).

18. As to claim 35, Blomgren et al. (750) taught that the computer further comprised processor register control circuitry designed to store information describing the decoding of the complex instructions into architecturally-visible processor registers of the computer (col. 7 lines 30-46).

19. As to claim 38, Blomgren et al. (009) taught that some instructions of the program were executed entirely in the software emulator, and some instructions were partially implemented in the hardware instruction decoder and partially implemented in the software emulator (col. 3 lines 57-67, see also Blomgren et al. (750) at col. 6 lines 33-45).

20. As to claim 52, Blomgren et al. (009) taught that the emulator was coded in an instruction set other than the instruction set decoded by the instruction decoder (col. 3 lines 57-60).

21. As to claims 53 and 54, Blomgren et al. (750) taught that entry to the software emulator was by exception inserted by the instruction decoder (col. 7 lines 29-54).

22. As to claim 55, Blomgren et al. (750) taught that the exceptions to enter the software

emulator used the same pipeline and architectural infrastructure as other exceptions raised by the instruction decoder or instruction execution unit (col. 7 lines 29-54).

23. As to claim 66, Blomgren et al. (750) taught that the instruction decoder was designed, when decoding an instruction to write multiple operands to memory, to keep intermediate state of the instruction in the inaccessible registers (col. 5 lines 55-67).

24. As to claim 67, Blomgren et al. (009) taught that the instruction decoder was designed to store a single datum in parts in two or more of the registers (fig. 6, col. 18 lines 56-60).

25. As to claim 68, Blomgren et al. (009) taught that the instruction decoder was designed to generate instructions to store a single datum in parts in a plurality of the inaccessible registers (fig. 6, col. 18 lines 56-60 and line 66 to col. 19 line 34).

26. As to claim 69, Blomgren et al. (009) taught that the instruction decoder was designed to generate an instruction to compute a condition value into a one of the inaccessible registers ("RES'VD") during execution of a single instruction (fig. 3, CR0, CR1, col. 7 lines 3-10 and 20-25).

27. As to claim 70, Blomgren et al. (009) taught that the instruction decoder was designed to generate an instruction to branch based on the condition value, and to leave the condition value dead before completion of the single instruction (col. 7 lines 55-61).

28. As to claim 71, Blomgren et al. (009) taught that the instruction decoder, general register file, and execution pipeline of the computer were cooperatively designed, such that execution of at least some single instructions results in computing multiple intermediate results being stored in a single inaccessible register (col. 17 lines 24-29, see also Blomgren et al. (750) at col. 5 lines 55-67).

29. As to claim 72, applicant has claimed how exceptions are inherently processed, in that the exception is processed before any side effects of the excepting instruction are committed to processor state.

30. Claims 9, 19, 22, and 24-27 are rejected under 35 USC 102(b) as being clearly anticipated by Hammond et al., U.S. Patent 5,638,525.

Hammond et al. was cited in applicant's information disclosure statement, paper number 2, received February 26, 2001.

Hammond et al. taught (e.g. see figs. 1-7) the invention as claimed (as per claim 9), including a data processing ("DP") system comprising:

30.1. a computer (fig. 1) comprising;

30.2. a RISC instruction decoder (fig. 6, 643) exposed for execution of user-state programs in a RISC instruction set (col. 2 lines 54-56), being an instruction set having fixed-length instructions and a load/store/operate organization (applicant has simply claimed the inherent definition of a RISC instruction set), and;

30.3. a CISC instruction decoder (641) exposed for execution by user-state programs in a CISC instruction set (col. 4 lines 50-51), being an instruction set with variable-length instructions and many instructions having multiple side-effects (col. 9 line 66 to col. 10 line 5); and,

30.4. an instruction execution pipeline (644) designed to execute the output of both the RISC instruction decoder and the CISC instruction decoder.

31. As to claim 19, Hammond et al. taught that the CISC instruction decoder (641) generates instructions (col. 16 lines 20-30) in the RISC instruction set (643) for execution by the instruction execution pipeline (644).

32. As to claim 22, Hammond et al. taught that the CISC instruction decoder was designed to generate multiple RISC instructions for parallel execution (Hammond et al. claim 7, part a).

33. As to claim 24, Hammond et al. taught that the CISC instruction decoder and instruction execution pipeline, with at most limited exceptions, was designed to independently complete the RISC instructions generated for CISC instructions once the CISC instructions are issued to the instruction execution pipeline (fig. 6, since the only source of instructions for the execution unit (644) is the RISC instruction decoder (643), the completion of those instructions is independent of the source of the instructions being the RISC decoder (643) or the CISC

decoder (641)).

34. As to claim 25, Hammond et al. taught that the instruction execution pipeline (fig. 6, 644), with at most limited exceptions, was designed to process the RISC instructions independently of whether the RISC instructions were decoded by the RISC instructions decoder or generated by the CISC instruction decoder (fig. 6, as the CISC instruction decoder (641) feeds directly into the RISC instruction decoder (643) and then into the execution unit (644), the execution unit is executing the instructions independently of which decoder actually decoded the instructions).

35. As to claim 26, as the claim is best under stood, Hammond et al. taught that the execution pipeline, with at most limited exceptions, was designed to process the RISC instructions independently [from] a point within a recipe of a CISC instruction at which the RISC instruction was generated (fig. 6, the CISC instructions are decoded into RISC instructions in box 641, so when they are decoded by box 643 and executed in box 644, they are independent of the point at which they were generated).

36. As to claim 27, Hammond et al. taught that the RISC (643) and CISC (641) instruction decoders were designed to emit RISC instructions (643, 644) to the instruction execution pipeline (644) in a unified format with identical operational codings, differing at most by a source designator (col. 16 lines 17-30).

37. Claims 20-21 are rejected under 35 USC § 103 as being unpatentable over Hammond et al., U.S. Patent 5,638,525, as applied to claims 9, 19, 22, and 24-27, supra., in view of Krishnaswamy, U.S. Patent 6,308,318.

38. As to claim 20, Hammond et al. did not teach that a RISC instruction translated from a CISC instruction carries a marker indicating it is a last RISC instruction for that CISC instruction. However, Krishnaswamy taught placing a marker at the end of a block of RISC instructions translated from CISC instructions to indicate a last RISC instruction (col. 2 lines 45-49). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have included Krishnaswamy's teachings into Hammond et al. because

of Krishnaswamy's teachings that the markings are necessary and required in a translation system in order to be able to process exceptions accurately (col. 1 lines 29-57 and col. 2 lines 26-40).

39. As to claim 21, Hammond et al. did not teach that a plurality of RISC instructions for a single CISC instruction contain markers indicating that the computer may accept an exception at the marked RISC instruction. However, Krishnaswamy taught having markers present (col. 2 lines 41-56) in a translated code stream (col. 1 lines 14-16 and 25-29) to indicate that the computer may accept exceptions at those points (col. 2 lines 25-57). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Krishnaswamy's markers with Hammond et al.'s translator because of Krishnaswamy teachings that it is required in a translation system to respond to exceptions that the state of the original source processor be recoverable in order to present and accurate and correct context to the exception handler (col. 1 lines 29-57, col. 2 lines 25-40).

40. Claims 5-7, 15-17, 23, 37, 45, 47-48, 50-51, and 64 are objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.

41. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

42. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

Richard Ellis
March 15, 2004